CUSTOMER NO. 34456

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellant(s):	Andrew W. Dornbusch et al.		
Title:	Integrated Circuit Suitable for Use in Radio Receivers		
App. No.:	10/691,212	Filed:	10/21/2003
Examiner:	CHU, Chris C.	Group Art Unit:	2815
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BOARD OF PATENT APPEALS
AND INTERFERENCES
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BRIEF IN SUPPORT OF APPEAL

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This brief contains these items under the following headings, and in the order set forth below (37 C.F.R. § 41.37(c)(1)):

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The final page of this brief before the beginning of the Appendix of Claims bears the agent's signature.

I. REAL PARTY IN INTEREST (37 C.F.R. § 41.37(c)(1)(i))

The real party in interest in this appeal is Silicon Laboratories Inc., the assignee in the entirety, as evidenced by the assignment recorded at Reel 014637, Frame 0952.

II. RELATED APPEALS AND INTERFERENCES (37 C.F.R. § 41.37(c)(1)(ii))

There are no interferences or other appeals that will directly affect, or be directly affected by, or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS (37 C.F.R. § 41.37(c)(1)(iii))

A. TOTAL NUMBER OF CLAIMS IN APPLICATION

There are twenty-six (26) claims pending in the application.

B. STATUS OF ALL THE CLAIMS

1. Claims pending:

   Claims 1, 3-8, 10-21, and 23-29.

2. Claims withdrawn from consideration but not canceled:

   NONE.

3. Claims allowed:

   NONE.

4. Claims objected to:

   NONE.

5. Claims rejected:

   Claims 1, 3-8, 10-21, and 23-29 are rejected under 35 U.S.C. § 112.

Claims 1, 3, 5-7, 15-19, 21, 23, 26, 27, and 29 are rejected under 35 U.S.C. § 102.

Claims 4, 8, 10-14, 20, 24, 25, and 28 are rejected under 35 U.S.C. § 103.

6. Claims canceled:

Claims 2, 9, 22, 30, and 31.

C. CLAIMS ON APPEAL

There are twenty-six (26) claims on appeal, claims 1, 3-8, 10-21, and 23-29.

IV. STATUS OF AMENDMENTS (37 C.F.R. § 41.37(c)(1)(iv))

No amendments have been submitted subsequent to the final Office Action mailed March 6, 2008 (hereinafter, "the Final Action").

V. SUMMARY OF THE CLAIMED SUBJECT MATTER (37 C.F.R. § 41.37(c)(1)(v))

The following summary is provided to give the Board the ability to quickly determine where the claimed subject matter appealed herein is described in the present application and is not to limit the scope of the claimed invention.

Independent claim 1 recites the features of an integrated circuit (e.g., integrated circuit 220, FIG. 2 and IC 500, FIG. 5) comprising: a semiconductor substrate (e.g., substrate 400, FIG. 4) having a first pair of bonding pads (e.g., output terminal 224, FIG. 2, bonding pads 442 and 444, FIG. 4, and para. 0021) for conducting a differential output signal thereon and configured to be coupled to an input of a first external filter (e.g., filter 112, FIG. 2), and a second pair of bonding pads (e.g., input terminal 226, FIG. 2, bonding pads 452 and 454, FIG. 4, and para. 0021) for conducting a differential input signal thereon and configured to be coupled to an output

of said first external filter; and an integrated circuit package (e.g., IC package 530, FIG. 5) encapsulating said semiconductor substrate (see, e.g., para. 0026) and having first and second terminal pairs (e.g., terminals 542 and 544 and terminals 552 and 554, FIG. 5) corresponding and coupled to said first and second pairs of bonding pads, respectively, wherein said first and second terminal pairs are separated by a first predetermined distance sufficient to maintain an input-to-output isolation attenuation therebetween (see, e.g., distance between terminal pair 542/544 and terminal pair 552/554, FIG. 5, and paras. 0023 and 0027-0031) of not less than a first stopband attenuation of the first external filter (see, e.g., paras. 0023 and 0027-0031).

Independent claim 15 recites the features of an integrated circuit (e.g., IC 500, FIG. 5) comprising: a semiconductor substrate (e.g., substrate 400, FIG. 4) having first, second, third, and fourth quadrants (e.g., quadrants 440, 450, 470, and 480, FIG. 4, and quadrants 540, 550, 570, and 580, FIG. 5) having respective first, second, third, and fourth bonding pads located therein (e.g., bonding pads 442, 444, 452, and 452, FIG. 4), said semiconductor substrate including a first circuit (e.g., a satellite receiver 430, FIG. 4) configured to be coupled to a first external filter (e.g., an external surface acoustic wave (SAW) filter, see para. 0024) coupled to said first circuit through said first and second bonding pads (e.g., bonding pads 442, 452, FIG. 4), and a second circuit (e.g., terrestrial receiver 470, FIG. 4) configured to be coupled to a second external filter (e.g., another external surface acoustic wave (SAW) filter, see paras. 0025 and 0026) coupled to said second circuit through said third and fourth bonding pads (e.g., bonding pads 472, 482, FIG. 4); and an integrated circuit package (e.g., IC package 530, FIG. 5) encapsulating said semiconductor substrate and having first, second, third, and fourth terminals (e.g., terminals 542, 552, 572, and 582, FIG. 5) corresponding and coupled to said first, second, third, and fourth bonding pads, respectively, wherein said first terminal and said second terminal

are separated by a first predetermined distance (see, e.g., distance between terminal 542 and terminal 552, FIG. 5 and paras. 0023 and 0027-0031) sufficient to maintain a first input-to-output isolation attenuation therebetween that is not less than a first stopband attenuation of the first external filter (see, e.g., paras. 0027-0030), and wherein said third terminal and said fourth terminal are separated by a second predetermined distance (see, e.g., distance between terminal 572 and terminal 582, FIG. 5 and paras. 0023 and 0027-0031) sufficient to maintain a second input-to-output isolation attenuation therebetween that is not less than a second stopband attenuation of the second external filter (see, e.g., paras. 0027-0030).

Independent claim 21 recites the features of an integrated circuit (e.g., integrated circuit 220, FIG. 2 and IC 500, FIG. 5) comprising: a semiconductor substrate (e.g., semiconductor substrate 400, FIG. 4) having a first pair of bonding pads (e.g., bonding pads 442, 444, FIG. 4) for conducting a differential output signal (e.g., SIFOP and SIFON, para. 0026) thereon and configured to be coupled to an input of an external filter (e.g., filter 112, FIG. 2), and a second pair of bonding pads (e.g., bonding pads 452, 454, FIG. 4) for conducting a differential input signal (e.g., SIFIP and SIFIN, para. 0026) thereon and configured to be coupled to an output of said external filter; and an integrated circuit package (e.g., IC package 530, FIG. 5) encapsulating said semiconductor substrate and having at least first and second sides (see, e.g., left and right side of IC package 530 as presented in FIG. 5), and comprising a first pair of terminals (e.g., terminals 542 and 544, FIG. 5) located at a first end of said first side and coupled to said first pair of bonding pads, and a second pair of terminals (e.g., terminals 552 and 554, FIG. 5) located at a second end of said first side opposite said first end (see layout of FIG. 5) and coupled to said second pair of bonding pads, wherein said first pair of terminals and said second pair of terminals are separated by a predetermined distance (see, e.g., distance between terminal

pair 542/544 and terminal pair 552/554, FIG. 5 and paras. 0023 and 0027-0031) sufficient to maintain an input-to-output isolation attenuation therebetween that not less than a stopband attenuation of said external filter (see, e.g., paras. 0023 and 0027-0031).

Independent claim 26 recites the features of an integrated circuit (e.g., IC 500, FIG. 5) comprising: adjacent first and second terminals (e.g., terminals 542, 544, FIG. 5) at a first end of a first side (see, e.g., top side of left side of IC 500 as presented in FIG. 5) of the integrated circuit configured to be coupled to a differential input of a first external filter (e.g., an external SAW filter, such as filter 112, see paras. 0025 and 0026); adjacent third and fourth terminals (e.g., terminals 552, 554, FIG. 5) at a second end of said first side (see, e.g., bottom end of left side of IC 500 as presented in FIG. 5) of the integrated circuit configured to be coupled to a differential output of said first external filter (see paras. 0025 and 0026), wherein said adjacent first and second terminals and said adjacent third and fourth terminals are separated by a first predetermined distance (see, e.g., distance between terminal pair 542/544 and terminal pair 552/554, FIG. 5 and paras. 0023 and 0027-0031) sufficient to maintain an input-to-output isolation attenuation therebetween that not less than a first stopband attenuation of said first external filter (see, e.g., paras. 0023 and 0027-0031); adjacent fifth and sixth terminals (e.g., terminals 572, 574, FIG. 5) at a first end of a second side (see, e.g., top end of right side of the IC 500 as presented in FIG. 5) of the integrated circuit configured to be coupled to a differential input of a second external filter (e.g., an external SAW filter, such as filter 112, see paras. 0025 and 0026); and adjacent seventh and eighth terminals (e.g., terminals 582, 584, FIG. 5) at a second end of said second side (see, e.g., bottom end of left side of the IC device 500 as presented in FIG. 5) of the integrated circuit configured to be coupled to a differential output of said second external filter, wherein said adjacent fifth and sixth terminals and said adjacent

seventh and eighth terminals are separated by a second predetermined distance (see, e.g., distance between terminal pair 572/574 and terminal pair 582/584, FIG. 5 and paras. 0023 and 0027-0031) sufficient to maintain an input-to-output isolation attenuation therebetween that is not less than a second stopband attenuation of said second external filter (see, e.g., paras. 0023 and 0027-0031).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL (37 C.F.R. § 41.37(c)(1)(vi))

A. Claims 1, 3-8, 10-21 and 23-29 are rejected under 35 U.S.C. § 112, second paragraph.

B. Claims 1, 3, 5-7, 21, and 23 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,396,154 (hereinafter, "Hikita").

C. Claims 15-19 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,576,589 (hereinafter, "Dreifus").

D. Claims 26, 27, and 29 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,296,391 (hereinafter, "Hazama").

E. Claims 4, 8, 10-14, 24, and 25 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Hikita.

F. Claim 20 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Dreifus in view of U.S. Patent No. 6,329,715 (hereinafter, "Hayashi").

G. Claim 28 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Hazama.

VII. ARGUMENTS (37 C.F.R. § 41.37(c)(1)(vii))

As illustrated by the arguments and issues below, each of the independent claims has a unique set of issues relating to its rejection and appeal. For purposes of this appeal, independent claims 1 and 21 and their dependent claims 8, 23, 24, and 25 stand or fall together, independent claim 15 and its dependent claims 16-20 stand or fall together, independent claim 26 and its dependent claims 27-29 stand or fall together, dependent claims 3, 4, 6, 7, 10, 11, 13, and 14 stand or fall together, and dependent claims 5 and 12 stand or fall together.

A. Rejection of Claims 1, 3-8, 10-21 and 23-29 under 35 U.S.C. § 112, 2nd Paragraph

At pages 2-5 of the Final Action, claims 1, 3-8, 10-21, and 23-29 were rejected under 35 U.S.C. § 112, second paragraph, as failing to particularly point out and distinctly claim the subject matter which the Applicants regard as the invention.

As stated by M.P.E.P. § 2173.02, the essential inquiry pertaining to this requirement is whether the claims set out and circumscribe a particular subject matter with a *reasonable degree* of clarity and particularity. Definiteness of claim language must be analyzed, not in a vacuum, but in light of: (A) The content of the particular application disclosure; (B) The teachings of the prior art; and (C) The claim interpretation that would be given by one possessing the ordinary level of skill in the pertinent art at the time the invention was made. As further stated by this section of the M.P.E.P., in reviewing a claim for compliance with 35 U.S.C. § 112, second paragraph, the examiner must consider the claim as a whole to determine whether the claim apprises one of ordinary skill in the art of its scope and, therefore, serves the notice function required by 35 U.S.C. § 112, second paragraph, by providing clear warning to others as to what constitutes infringement of the patent. *See, e.g., Solomon v. Kimberly-Clark Corp.*, 216 F.3d

1372, 1379, 55 USPQ2d 1279, 1283 (Fed. Cir. 2000). *See also Metabolite Labs., Inc. v. Lab. Corp. of Am. Holdings*, 370 F.3d 1354, 1366, 71 USPQ2d 1081, 1089 (Fed. Cir. 2004) ("The requirement to 'distinctly' claim means that the claim must have a meaning discernible to one of ordinary skill in the art when construed according to correct principles...Only when a claim remains insolubly ambiguous without a discernible meaning after all reasonable attempts at construction must a court declare it indefinite."). Accordingly, a claim term that is not used or defined in the specification is not indefinite if the meaning of the claim term is discernible. *Bancorp Services, L.L.C. v. Hartford Life Ins. Co.*, 359 F.3d 1367, 1372, 69 USPQ2d 1996, 1999-2000 (Fed. Cir. 2004). If the language of the claim is such that a person of ordinary skill in the art could not interpret the metes and bounds of the claim so as to understand how to avoid infringement, a rejection of the claim under 35 U.S.C. § 112, second paragraph, would be appropriate. See *Morton Int'l, Inc. v. Cardinal Chem. Co.*, 5 F.3d 1464, 1470, 28 USPQ2d 1190, 1195 (Fed. Cir. 1993).

With respect to the claims, the Office objects to the claim language "wherein said first and second terminal pairs are separated by a first predetermined distance sufficient to maintain an input-to-output isolation attenuation therebetween of not less than a first stopband attenuation of the first external filter" and similar claim language. *Final Action*, p. 2. In particular, the Office objects to the claim phrase "not less than a first stopband attenuation of the first external filter" as failing to define the metes and bounds of the claims. The Office's rationale for this rejection is that because 1) "the stopband attenuation specifies the minimum amount of **attenuation** a filter will exhibit at a designated frequency or range of frequencies, which lie outside the pass band" and 2) the claim fails to recite "a specific number of the first stopband attenuation nor [whether it] is a positive or negative integer number", "any attenuation between

negative infinity numbers and positive infinity numbers could read as the first stopband attenuation of the first external filter." *Final Action*, p. 3 (emphasis in original). On the basis of this rationale, the Office asserts that the claims will need to recite particular values for the first stopband attenuation and the "first predetermined distance" (and similar claim language) in order to be rendered definite. *Id*.

With respect to the Office's reasoning that the first stopband attenuation of the external filter could be between negative and positive infinity and thus is unclear, it is submitted that no actual filter in application has an infinite attenuation, much less an infinite stopband attenuation. Moreover, the Office has failed to provide any evidence of an actual filter having infinite stopband attenuation. As noted above, the standard for evaluating a claim under § 112, second paragraph, is whether the claim apprises *one of ordinary skill in the art* of its scope. As one of ordinary skill in the art would readily appreciate that the Office's purely hypothetical example of a filter with an infinite stopband attenuation does not and will not exist in practice, one of ordinary skill in the art will readily appreciate that the stopband attenuation recited in the claim language is a finite attenuation, and thus definite and unambiguous. That is, one of ordinary skill in the art, having selected an external filter, can readily determine the finite stopband attenuation of the selected filter using any of a variety of well-known techniques and further can readily determine whether the input-to-output isolation attenuation afforded by the distance between the bonding pads/terminal pairs of the IC device is not less than this stopband attenuation. Thus, one of ordinary skill in the art, using the language of the claims, can readily understand how to avoid infringement based on the relationship between the determined stopband attenuation and the determined isolation attenuation.

With respect to the Office's reasoning that the claims need to recite particular values for the recited "stopband attenuation" and the recited "predetermined distance" in order to be rendered definite, it appears that the Office is attempting to set a higher standard than the standard of a "*reasonable degree* of clarity and particularity" established by the M.P.E.P and the judiciary. *See, e.g., M.P.E.P.* § 2172.03 ("the essential inquiry pertaining to [§ 112, second paragraph] is whether the claims set out and circumscribe a particular subject matter with a *reasonable degree* of clarity and particularity")(emphasis added). The recitation of a particular number or range of numbers is not required for a "reasonable degree of clarity and particularity." Rather, as noted above, the stopband attenuation is defined by the particular external filter selected for implementation, and thus one of ordinary skill in the art will readily appreciate that a selected external filter for which the first pair of bonding pads are configured to be coupled to (as recited by the claims) will have a particular finite, measurable stopband attenuation and the particular distance between the bonding pads/terminal pairs of the IC will result in a particular, finite isolation attenuation, and the potential for infringement in view of these determined characteristics is reasonably discerned from the language of the claims. Accordingly, it is respectfully submitted that the language of the claims is clear and sufficiently defines the metes and bounds of the claimed subject matter.

For at least the reasons provided above, the claims particularly point out and distinctly claim the subject matter regarded as the invention. Claims 1, 3-8, 10-21, and 23-29 therefore are consistent with the requirements of 35 U.S.C. § 112, second paragraph.

B. Rejection of Claims 1, 3, 5-7, 21, and 23 under 35 U.S.C. § 102(b)

In Section 3 of the Final Action, claims 1, 3, 5-7, 21, and 23 were rejected under 35 U.S.C. § 102(b) as anticipated by Hikita. As stated by M.P.E.P. § 706.02, "for anticipation under 35 U.S.C. 102, the reference must teach every aspect of the claimed invention either explicitly or impliedly. Any feature not directly taught must be inherently present." The Office bears the burden of presenting at least a *prima facie* case of anticipation. *In re Sun*, 31 USPQ2d 1451, 1453 (Fed. Cir. 1993) (unpublished).

For ease of reference, independent claims 1 and 21 are reproduced in their entireties below:

1. (Previously Presented) An integrated circuit comprising:

a semiconductor substrate having a first pair of bonding pads for conducting a differential output signal thereon and configured to be coupled to an input of a first external filter, and a second pair of bonding pads for conducting a differential input signal thereon and configured to be coupled to an output of said first external filter; and

an integrated circuit package encapsulating said semiconductor substrate and having first and second terminal pairs corresponding and coupled to said first and second pairs of bonding pads, respectively,

wherein said first and second terminal pairs are separated by a first predetermined distance sufficient to maintain an input-to-output isolation attenuation therebetween of not less than a first stopband attenuation of the first external filter.

21. (Previously Presented) An integrated circuit comprising:

a semiconductor substrate having a first pair of bonding pads for conducting a differential output signal thereon and configured to be coupled to an input of an external filter, and a second pair of bonding pads for conducting a differential input signal thereon and configured to be coupled to an output of said external filter; and

an integrated circuit package encapsulating said semiconductor substrate and having at least first and second sides, and comprising a first pair of terminals located at a first end of said first side and coupled to said first pair of bonding pads, and a second pair of terminals located at a second end of said first side opposite said first end and coupled to said second pair of bonding pads, wherein said first pair of terminals and said second pair of terminals are separated by a predetermined distance sufficient to maintain an input-to-output isolation attenuation therebetween that not less than a stopband attenuation of said external filter.

a) Hikita fails to disclose a stopband attenuation, a predetermined distance sufficient to maintain an input-to-output isolation attenuation between first and second terminal pair, or any relationship between the two as provided by claims 1 and 21

Independent claim 1 recites the features of "wherein said first and second terminal pairs are *separated by a first predetermined distance sufficient to maintain an input-to-output isolation attenuation therebetween* of not less than *a first stopband attenuation of the first external filter*" and independent claim 21 recites similar features. Hikita fails to contemplate a stopband attenuation of an external filter, or any other operational attenuation for that matter. Further, Hikita fails to disclose or suggest a *predetermined* distance sufficient to maintain an input-to-output isolation attenuation that is not less than the stopband attenuation of an external filter, much less that first and second terminal pairs of an integrated circuit are separated by such predetermined distance as provided by claims 1 and 21. In response, the Office contends that

> the first stopband attenuation could be any number between negative infinity numbers and positive infinity numbers [sic]. If we measure a stopband attenuation of any filter at one point that is the lowest value of the operational attenuation of the filter and measure the input-to-output isolation attenuation at it's highest point, then the value of the input-to-output isolation is always greater [than] the lowest value of the stopband attenuation of any filter. Since Hikita et al. discloses a filter, [...] Hikita et al. fully anticipates [the above recited claim features].

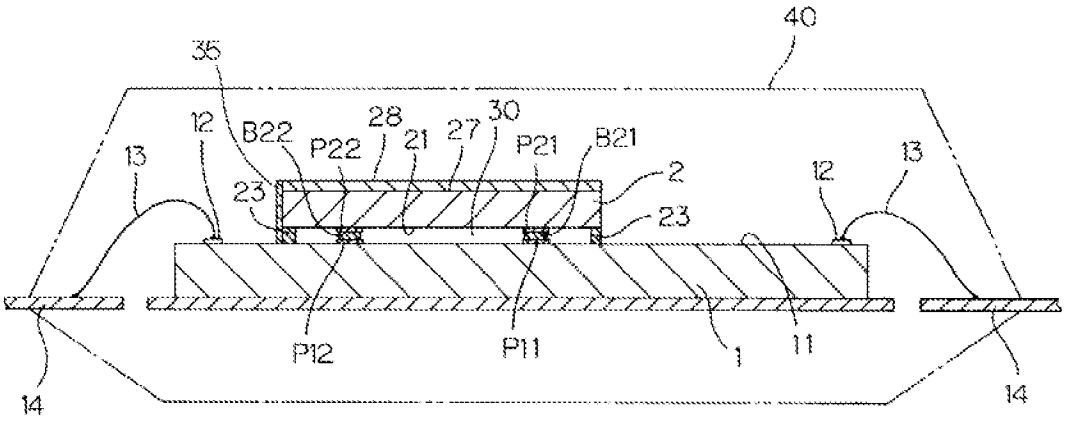
Final Action, p. 6.

As noted above, one of ordinary skill in the art will appreciate that an external filter does not have an infinite stopband attenuation, but rather a finite and measurable attenuation. As also noted above, the input-to-output isolation attenuation between terminal pairs of an integrated circuit is finite and measurable or estimable and is based on the distance between the terminal pairs. Thus, contrary to the Office's assertions, the input-to-output isolation between terminal pairs is not "always greater" than the stopband attenuation of an external filter. Hikita fails to contemplate an external filter, a stopband attenuation of an external filter, an input-to-output isolation attenuation between terminal pairs, how such input-to-output isolation attenuation is affected by distance, or a predetermined distance between the terminal pairs to achieve any particular input-to-output isolation attenuation in any manner, so Hikita necessarily fails to disclose or even suggest that an integrated circuit having terminal pairs configured to be coupled to an external filter via terminal pairs has those terminal pairs separated by a *predetermined* distance sufficient to maintain an input-to-output isolation attenuation therebetween of not less than the stopband attenuation of an external filter as provided by claims 1 and 21.

b) Hikita fails to disclose an integrated circuit package encapsulating a semiconductor substrate and having first and second terminal pairs corresponding and coupled to first and second pairs of bonding pads configured to be coupled to an external filter as recited by claim 1

Independent claim 1 recites the features "a semiconductor substrate having a first pair of bonding pads for conducting a differential output signal thereon and configured to be coupled to an input of a first external filter, and a second pair of bonding pads for conducting a differential input signal thereon and configured to be coupled to an output of said first external filter" and "an integrated circuit package encapsulating said semiconductor substrate and having first and second terminal pairs corresponding and coupled to said first and second pairs of bonding pads,

respectively." The Office identifies the surface acoustic wave (SAW) filter 22 and the package 40 of FIG. 2 of Hikita as disclosing the claimed "external filter" and "integrated circuit package," respectively. *Final Action*, p. 2. For ease of reference, FIG. 2 of Hikita is reproduced below:



Hikita, FIG. 2

As illustrated by FIG. 2 and the passage of Hikita at page 3, line 46 – page 4, line 46, Hikita teaches that the disclosed device has a chip-on-chip structure whereby the connection pads P11, P12, P13, P14, and P15 of the mother chip 1 (which implements "functional elements such as transistors") and connection pads P21, P22, P23, and P24 of the daughter chip 2 (in which the SAW filter 22 is implemented) are joined together. As illustrated by FIG. 2, this structure results in the mother chip 1 and the daughter chip 2 being encapsulated by the package 40. The only structure of the package 40 that could constitute a terminal is the lead frame 14 that is connected to the mother chip 1 via bonding wires 13. However, the lead frame 14 does not "correspond to" the connection pads of the daughter chip 2 implementing the SAW filter 22, nor does Hikita disclose that the lead frame 14 is coupled to the connection pads of the SAW filter 22 in any manner. Thus, Hikita fails to disclose or suggest the recited features of an integrated

circuit package . . . having first and second terminal pairs corresponding and coupled to said first and second pairs of bonding pads, respectively" as recited by claim 1.

c) Hikita fails to disclose an integrated circuit package encapsulating a semiconductor substrate and comprising a first pair of terminals coupled to a first pair of bonding pads configured to be coupled to an input of an external filter and comprising a second pair of terminals coupled to a second pair of bonding pads configured to be coupled to an output of the external filter as recited by claim 21

Independent claim 21 recites the features of "a semiconductor substrate having a first pair of bonding pads for conducting a differential output signal thereon and configured to be coupled to an input of an external filter, and a second pair of bonding pads for conducting a differential input signal thereon and configured to be coupled to an output of said external filter" and "an integrated circuit package encapsulating said semiconductor substrate . . . and comprising a first pair of terminals located at a first end of said first side and coupled to said first pair of bonding pads, and a second pair of terminals located at a second end of said first side opposite said first end and coupled to said second pair of bonding pads. As discussed above, Hikita discloses that the mother chip 1 and the daughter chip 2 (which implements the SAW filter 22) are internally bonded and Hikita fails to disclose any terminal of the package 40 that is coupled to the "connection pads" of the daughter chip 2. Further, even if it were assumed, *arguendo*, that the lead frame 14 of Hikita somehow was coupled to the "connection pads" of the daughter chip 2, Hikita fails to disclose that the pairs of leads coupled to the connection pads that serve as the input of the SAW filter 22 and the pair of leads coupled to the connection pads that serve as the output of the SAW filter 22 are located at different ends of a side of the package 400 as provided by claim 21. Hikita therefore fails to disclose the first and second pairs of terminals recited by claim 21.

d) Hikita fails to disclose first and second terminal pairs separated by a first plurality of intervening terminals as recited by claims 3 and 10

Dependent claim 3 recites the additional features of "wherein said first and second terminal pairs are . . . separated by a first plurality of intervening terminals" and dependent claim 10 recites similar features. As discussed above, Hikita fails to disclose the recited first and second terminal pairs, and thus Hikita necessarily fails to disclose that such first and second terminal pairs are separated by a plurality of intervening terminals as provided by claims 3 and 10.

e) Claims 1, 3, 5-7, 21, and 23 are allowable under 35 U.S.C. § 102(b)

For at least the reasons provided above, Hikita fails to disclose each and every feature recited by claims 1 and 21, and thus also fails to disclose each and every feature recited by dependent claims 3, 5-7, and 23. Accordingly, the Office fails to establish a sufficient showing of anticipation in support of its rejection of claims 1, 3, 5-7, 21, and 23. Claims 1, 3, 5-7, 21, and 23 therefore are allowable under 35 U.S.C. § 102(b).

C. Rejection of Claims 15-19 under 35 U.S.C. § 102(b)

In Section 6 of the Final Action, claims 15-19 were rejected under 35 U.S.C. § 102(b) as anticipated by Dreifus.

For ease of reference, independent claim 15 is reproduced in its entirety below:

15. (Previously Presented) An integrated circuit comprising:
a semiconductor substrate having first, second, third, and fourth quadrants having respective first, second, third, and fourth bonding pads located therein, said semiconductor substrate including a first circuit configured to be coupled to a first external filter coupled to said first circuit through said first and second bonding

pads, and a second circuit configured to be coupled to a second external filter coupled to said second circuit through said third and fourth bonding pads; and

an integrated circuit package encapsulating said semiconductor substrate and having first, second, third, and fourth terminals corresponding and coupled to said first, second, third, and fourth bonding pads, respectively, wherein said first terminal and said second terminal are separated by a first predetermined distance sufficient to maintain a first input-to-output isolation attenuation therebetween that is not less than a first stopband attenuation of the first external filter, and wherein said third terminal and said fourth terminal are separated by a second predetermined distance sufficient to maintain a second input-to-output isolation attenuation therebetween that is not less than a second stopband attenuation of the second external filter.

a) Dreifus fails to disclose a stopband attenuation, a predetermined distance sufficient to maintain an input-to-output isolation attenuation between terminals, or any relationship between the two as provided by claim 15

Independent claim 15 recites the features of "wherein said first terminal and said second terminal are separated by a first *predetermined* distance sufficient to maintain a first input-to-output isolation attenuation therebetween that is not less than a first stopband attenuation of the first external filter, and wherein said third terminal and said fourth terminal are separated by a second *predetermined* distance sufficient to maintain a second input-to-output isolation attenuation therebetween that is not less than a second stopband attenuation of the second external filter." Dreifus fails to contemplate an operational attenuation of an external filter in any manner, much less a stopband attenuation. Dreifus also fails to disclose or suggest that first and second terminals of an integrated circuit are separated by a *predetermined* distance sufficient to maintain an input-to-output isolation attenuation therebetween that is not less than a stopband attenuation of an external filter as provided by claim 15.

The Office responds by asserting the same rationale asserted under Hikita, namely that the measured input-to-output isolation attenuation will always be greater than the lowest measured operational isolation of an external filter. As discussed above, this rationale finds no support in the disclosures of Dreifus or the knowledge of one of ordinary skill in the art, particularly with respect to the stopband attenuation of an external filter, and therefore fails to support an assertion that Dreifus discloses or suggests the features of "wherein said first terminal and said second terminal are separated by a first *predetermined* distance sufficient to maintain a first input-to-output isolation attenuation therebetween that is not less than a first stopband attenuation of the first external filter, and wherein said third terminal and said fourth terminal are separated by a second predetermined distance sufficient to maintain a second input-to-output isolation attenuation therebetween that is not less than a second stopband attenuation of the second external filter" as recited by claim 15.

b) Dreifus fails to disclose an integrated circuit package encapsulating a semiconductor substrate and having first, second, third, and fourth terminals corresponding and coupled to first, second, third, and fourth bonding pad as recited by claim 15

Independent claim 15 recites the features of "a semiconductor substrate having first, second, third, and fourth quadrants having respective first, second, third, and fourth bonding pads located therein, said semiconductor substrate including a first circuit configured to be coupled to a first external filter coupled to said first circuit through said first and second bonding pads, and a second circuit configured to be coupled to a second external filter coupled to said second circuit through said third and fourth bonding pads" and "an integrated circuit package encapsulating said semiconductor substrate and having first, second, third, and fourth terminals corresponding and coupled to said first, second, third, and fourth bonding pads, respectively." The Office asserts that the recited "integrated circuit package" is met by the passage of Dreifus at col. 6, lines 33 and 34 and by FIG. 2 of Dreifus. *Final Action*, p. 10. FIG. 2 of Dreifus fails to disclose an integrated circuit package and the cited passage at col. 6, lines 33 and 34 of Dreifus merely states "[c]ontact pads 26 (FIG. 2) facilitate external connection to the interdigitated electrodes 24." Facilitation of "external connection" does not expressly or inherently disclose an integrated circuit package that encapsulates the substrate of Dreifus, much less that any such integrated circuit package necessarily includes terminals coupled to the contact pads 26 of Dreifus. Dreifus therefore fails to disclose an "integrated circuit package encapsulating the semiconductor substrate" as recited by claim 15.

c) Claims 15-19 are allowable under 35 U.S.C. § 102(b)

For at least the reasons provided above, Dreifus fails to disclose each and every feature recited by claim 15, and thus also fails to disclose each and every feature recited by dependent

claims 16-19. Accordingly, the Office fails to establish a sufficient showing of anticipation in support of its rejection of claims 15-19. Claims 15-19 therefore are allowable under 35 U.S.C. § 102(b).

D. Rejection of Claims 26, 27, and 29 under 35 U.S.C. § 102(b)

In Section 7 of the Final Action, claims 26, 27, and 29 were rejected under 35 U.S.C. § 102(b) as anticipated by Hazama.

For ease of reference, independent claim 26 is reproduced in its entirety below:

26. (Previously Presented) An integrated circuit comprising:

adjacent first and second terminals at a first end of a first side of the integrated circuit configured to be coupled to a differential input of a first external filter;

adjacent third and fourth terminals at a second end of said first side of the integrated circuit configured to be coupled to a differential output of said first external filter, wherein said adjacent first and second terminals and said adjacent third and fourth terminals are separated by a first predetermined distance sufficient to maintain an input-to-output isolation attenuation therebetween that not less than a first stopband attenuation of said first external filter;

adjacent fifth and sixth terminals at a first end of a second side of the integrated circuit configured to be coupled to a differential input of a second external filter; and

adjacent seventh and eighth terminals at a second end of said second side of the integrated circuit configured to be coupled to a differential output of said second external filter, wherein said adjacent fifth and sixth terminals and said adjacent seventh and eighth terminals are separated by a second predetermined distance sufficient to maintain an input-to-output isolation attenuation therebetween that is not less than a second stopband attenuation of said second external filter.

a) Hazama fails to disclose a stopband attenuation, a predetermined distance sufficient to maintain an input-to-output isolation attenuation between terminals, or any relationship between the two as provided by claim 26

Independent claim 26 recites the features of "wherein said adjacent first and second terminals and said adjacent third and fourth terminals are separated by a first predetermined distance sufficient to maintain an input-to-output isolation attenuation therebetween that not less than a first stopband attenuation of said first external filter" and "wherein said adjacent fifth and sixth terminals and said adjacent seventh and eighth terminals are separated by a second predetermined distance sufficient to maintain an input-to-output isolation attenuation therebetween that is not less than a second stopband attenuation of said second external filter." Hazama fails to contemplate an operational attenuation of an external filter in any manner, much less a stopband attenuation. Hazama also fails to disclose or suggest that pairs of terminals of an integrated circuit are separated by a *predetermined* distance sufficient to maintain an input-to-output isolation attenuation therebetween that is not less than a stopband attenuation of an external filter as provided by claim 26.

The Office responds by asserting the same rationale asserted under Hikita and Dreifus, namely that the measured input-to-output isolation attenuation will always be greater than the lowest measured operational isolation of an external filter. This rationale finds no support in the disclosures of Hazama or the knowledge of one of ordinary skill in the art, particularly with respect to the stopband attenuation of an external filter, and therefore fails to support an assertion that Hazama discloses the above-identified features recited by claim 26.

b) Claims 26, 27, and 29 are allowable under 35 U.S.C. § 102(b)

For at least the reasons provided above, Hazama fails to disclose each and every feature recited by claim 26, and thus also fails to disclose each and every feature recited by dependent claims 27 and 29. Accordingly, the Office fails to establish a sufficient showing of anticipation in support of its rejection of claims 26, 27, and 29. Claims 26, 27, and 29 therefore are allowable under 35 U.S.C. § 102(b).

E. Rejection of Claims 4, 8, 10-14, 24 and 25 under 35 U.S.C. § 103(a)

In Section 9 of the Final Action, claims 4, 8, 10-14, and 25 were rejected under 35 U.S.C. § 103(a) as unpatentable over Hikita.

a) Hikita fails to disclose or suggest each and every feature recited by claims 1 and 21, from which claims 4, 8, 10-14, and 25 respectively depend

Claims 4, 8, and 10-14 depend from claim 1 and claims 24 and 25 depend from claim 21. As discussed above, Hikita fails to disclose a number of features recited by claims 1 and 21. Hikita in fact also fails to suggest these missing features, and the Office fails to provide an explicit analysis with an articulated reasoning to address how one of ordinary skill in the art might arrive at these features missing from the disclosure of Hikita. *See KSR International Co. v. Teleflex Inc.*, 550 U.S. ___, ___, 127 S. Ct. 1727, 1741 (2007). Hikita therefore fails to disclose or suggest the particular combinations of features recited by claims 4, 8, 10-14, 24 and 25 at least by virtue of their respective dependencies from one of claims 1 and 21.

b) Hikita fails to disclose or suggest a plurality of intervening terminals including a power supply terminal as recited by claims 5 and 12

Claim 5 depends from claim 3 and claim 12 depends from claim 10. As discussed above, Hikita fails to disclose, or even suggest, first and second terminal pairs of an integrated circuit package that are coupled to first and second bonding pads configured to be coupled to an external filter as recited by claim 1, or that the first and second terminal pairs are separated by a first plurality of intervening terminals as recited by dependent claims 3 and 10. Hikita therefore necessarily fails to disclose or suggest that the first plurality of intervening terminals "comprises at least one power supply terminal" as recited by claims 5 and 12.

c) Claims 4, 8, 10-14, 24 and 25 are allowable under 35 U.S.C. § 103(a)

For at least the reasons provided above, Hikita fails to disclose or suggest each and every feature recited by claims 4, 8, 10-14, 24 and 25, and claims 4, 8, 10-14, 24 and 25 would not have been obvious to one of ordinary skill in the art in view of Hikita. Accordingly, the Office fails to establish a sufficient showing of obviousness in support of its rejection of claims 4, 8, 10-14, 24 and 25. Claims 4, 8, 10-14, 24 and 25 therefore are allowable under 35 U.S.C. § 103(a).

F. Rejection of Claim 20 under 35 U.S.C. § 103(a)

In Section 10 of the Final Action, claim 20 was rejected under 35 U.S.C. § 103(a) as unpatentable over Dreifus in view of Hayashi. Claim 20 depends from claim 15. As discussed above, Dreifus fails to disclose a number of features recited by claim 15. Hayashi fails to compensate for the deficiencies of Dreifus with respect to claim 15, and the Office fails to provide an explicit analysis with an articulated reasoning to address how one of ordinary skill in the art might arrive at these features missing from the combination of Dreifus and Hayashi.

Accordingly, the proposed combination of Dreifus and Hayashi fails to disclose or suggest each and every feature recited by claims 20 at least by virtue of its dependency from claim 15. Claim 20 therefore is allowable under 35 U.S.C. § 103(a).

G. Rejection of Claim 28 under 35 U.S.C. § 103(a)

In Section 11 of the Final Action, claim 28 was rejected under 35 U.S.C. § 103(a) as unpatentable over Hazama. Claim 28 depends from claim 26. As discussed above, Hazama fails to disclose a number of features recited by claim 26. Hazama in fact also fails to suggest these missing features, and the Office fails to provide an explicit analysis with an articulated reasoning to address how one of ordinary skill in the art might arrive at these features missing from the disclosure of Hikita. Hazama therefore fails to disclose or suggest the particular combinations of features recited by claim 28 at least by virtue of its dependency from claim 26. Claim 28 therefore is allowable under 35 U.S.C. § 103(a).

VIII. CONCLUSION

For at least the reasons given above, all pending claims are allowable and the Appellants therefore respectfully requests reconsideration and allowance of all claims and that this patent application be passed to issue.

Respectfully submitted,

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Date

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IX. APPENDIX OF CLAIMS INVOLVED IN THE APPEAL (37 C.F.R. § 41.37(c)(1)(viii))

The text of each claim involved in the appeal is as follows:

1. (Previously Presented) An integrated circuit comprising:

a semiconductor substrate having a first pair of bonding pads for conducting a differential output signal thereon and configured to be coupled to an input of a first external filter, and a second pair of bonding pads for conducting a differential input signal thereon and configured to be coupled to an output of said first external filter; and

an integrated circuit package encapsulating said semiconductor substrate and having first and second terminal pairs corresponding and coupled to said first and second pairs of bonding pads, respectively,

wherein said first and second terminal pairs are separated by a first predetermined distance sufficient to maintain an input-to-output isolation attenuation therebetween of not less than a first stopband attenuation of the first external filter.

2. (Canceled)

3. (Previously Presented) The integrated circuit of claim 1, wherein said first and second terminal pairs are located along a first side of said integrated circuit package and separated by a first plurality of intervening terminals.

4. (Previously Presented) The integrated circuit of claim 3, wherein said first plurality of intervening terminals comprises twelve terminals.

5. (Previously Presented) The integrated circuit of claim 3, wherein said first plurality of intervening terminals comprises at least one power supply terminal.

6. (Previously Presented) The integrated circuit of claim 3, wherein first and second terminals of said first terminal pair are adjacent to one another, and first and second terminals of said second terminal pair are adjacent to one another.

7. (Previously Presented) The integrated circuit of claim 6, wherein said first and second terminal pairs are located at opposite ends of said first side of said integrated circuit package.

8. (Previously Presented) The integrated circuit of claim 1, wherein:

said semiconductor substrate further has a third pair of bonding pads conducting a differential output signal thereon and configured to be coupled to an input of a second external filter, and a fourth pair of bonding pads conducting a differential input signal thereon and configured to be coupled to an output of said second external filter;

said integrated circuit package further has third and fourth terminal pairs corresponding and coupled to said third and fourth pairs of bonding pads, respectively; and

said third and fourth terminal pairs are separated by a second predetermined distance sufficient to maintain an input-to-output isolation attenuation therebetween of not less than a second stopband attenuation of said second external filter.

9. (Canceled)

10. (Previously Presented) The integrated circuit of claim 8, wherein said first and second terminal pairs are located along a first side of said integrated circuit package and separated by a first plurality of intervening terminals and said third and fourth terminal pairs are located along a second side of said integrated circuit package and separated by a second plurality of intervening terminals.

11. (Previously Presented) The integrated circuit of claim 10, wherein said first and second pluralities of intervening terminals each comprises twelve terminals.

12. (Previously Presented) The integrated circuit of claim 10, wherein said first and second pluralities of intervening terminals each comprises at least one power supply terminal.

13. (Previously Presented) The integrated circuit of claim 10, wherein first and second terminals of each of said first, second, third, and fourth terminal pairs are adjacent to one another.

14. (Previously Presented) The integrated circuit of claim 10, wherein said first and second terminal pairs are located at opposite ends of said first side of said integrated circuit package and said third and fourth terminal pairs are located at opposite ends of said second side of said integrated circuit package.

15. (Previously Presented) An integrated circuit comprising:

a semiconductor substrate having first, second, third, and fourth quadrants having respective first, second, third, and fourth bonding pads located therein, said semiconductor substrate including a first circuit configured to be coupled to a first external filter coupled to said first circuit through said first and second bonding pads, and a second circuit configured to be coupled to a second external filter coupled to said second circuit through said third and fourth bonding pads; and

an integrated circuit package encapsulating said semiconductor substrate and having first, second, third, and fourth terminals corresponding and coupled to said first, second, third, and fourth bonding pads, respectively, wherein said first terminal and said second terminal are separated by a first predetermined distance sufficient to maintain a first input-to-output isolation attenuation therebetween that is not less than a first stopband attenuation of the first external filter, and wherein said third terminal and said fourth terminal are separated by a second predetermined distance sufficient to maintain a second input-to-output isolation attenuation therebetween that is not less than a second stopband attenuation of the second external filter.

16. (Previously Presented) The integrated circuit of claim 15, wherein said first and second circuits comprise portions of radio frequency (RF) receivers.

17. (Previously Presented) The integrated circuit of claim 16, wherein said first circuit comprises a portion of a satellite receiver and said second circuit comprises a portion of a terrestrial receiver.

18. (Previously Presented) The integrated circuit of claim 16, wherein said first and second circuits have substantially the same layout.

19. (Previously Presented) The integrated circuit of claim 15, wherein said first and second circuits are configured to be coupled to first and second external surface acoustic wave (SAW) filters, respectively.

20. (Previously Presented) The integrated circuit of claim 15, wherein said semiconductor substrate further comprises fifth, sixth, seventh, and eighth bonding pads respectively located in said first, second, third, and fourth quadrants and forming complementary signal pairs with signals conducted on said first, second, third, and fourth bonding pads, respectively.

21. (Previously Presented) An integrated circuit comprising:

a semiconductor substrate having a first pair of bonding pads for conducting a differential output signal thereon and configured to be coupled to an input of an external filter, and a second pair of bonding pads for conducting a differential input signal thereon and configured to be coupled to an output of said external filter; and

an integrated circuit package encapsulating said semiconductor substrate and having at least first and second sides, and comprising a first pair of terminals located at a first end of said first side and coupled to said first pair of bonding pads, and a second pair of terminals located at a second end of said first side opposite said first end and coupled to said second pair of bonding pads, wherein said first pair of terminals and said second pair of terminals are separated by a predetermined distance sufficient to maintain an input-to-output isolation attenuation therebetween that not less than a stopband attenuation of said external filter.

22. (Canceled)

23. (Previously Presented) The integrated circuit of claim 21, wherein said integrated circuit package further comprises a thin quad flat package (TQFP).

24. (Previously Presented) The integrated circuit of claim 23, wherein said integrated circuit package further comprises a 64-lead TQFP.

25. (Previously Presented) The integrated circuit of claim 21, wherein said semiconductor substrate further has a third pair of bonding pads conducting a second differential output signal thereon and configured to be coupled to an input of a second external filter, and a fourth pair of bonding pads conducting a second differential input signal thereon and configured to be coupled to an output of said second external filter, and said integrated circuit package further has a third pair of terminals located on a first end of said second side and coupled to said third pair of bonding pads, and a fourth pair of terminals located on a second end of said second side opposite said first end and coupled to said fourth pair of bonding pads.

26. (Previously Presented) An integrated circuit comprising:

adjacent first and second terminals at a first end of a first side of the integrated circuit configured to be coupled to a differential input of a first external filter;

adjacent third and fourth terminals at a second end of said first side of the integrated circuit configured to be coupled to a differential output of said first external filter, wherein said adjacent first and second terminals and said adjacent third and fourth terminals are separated by a first predetermined distance sufficient to maintain an input-to-output isolation attenuation therebetween that not less than a first stopband attenuation of said first external filter;

adjacent fifth and sixth terminals at a first end of a second side of the integrated circuit configured to be coupled to a differential input of a second external filter; and

adjacent seventh and eighth terminals at a second end of said second side of the integrated circuit configured to be coupled to a differential output of said second external filter, wherein said adjacent fifth and sixth terminals and said adjacent seventh and eighth terminals are separated by a second predetermined distance sufficient to maintain an input-to-output isolation attenuation therebetween that is not less than a second stopband attenuation of said second external filter.

27. (Previously Presented) The integrated circuit of claim 26, wherein the integrated circuit comprises a quad flat package.

28. (Previously Presented) The integrated circuit of claim 27, wherein said quad flat package comprises sixty four terminals having corresponding pin numbers assigned consecutively around a periphery of said quad flat package starting from a pin one corner, and wherein said first and second terminals correspond to pins one and two, said third and fourth terminals correspond to pins fifteen and sixteen, said fifth and sixth terminals correspond to pins forty seven and forty eight, and said seventh and eighth terminals correspond to pins thirty three and thirty four.

29. (Previously Presented) The integrated circuit of claim 26, wherein each of said first and second external filters comprises a surface acoustic wave (SAW) filter.

30. (Canceled)

31. (Canceled)

X. EVIDENCE APPENDIX (37 C.F.R. § 41.37(c)(1)(ix))

NONE.

XI. RELATED PROCEEDINGS APPENDIX (37 C.F.R. § 41.37(c)(1)(x))

NONE.